DTM64312E

2GB - 240-Pin 2Rx8 Registered ECC DDR3 DIMM

DR DATARAM
Optimizing Value and Performance

Identification

DTM64312E 256Mx72
2GB 2Rx8 PC3-10600R-9-10-B0

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

667 MHz / PC3-10600 / 9-9-9
533 MHz / PC3-8500 / 8-8-8
400 MHz / PC3-6400 / 6-6-6

Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: 1.5V ± 0.075

I/O Type: SSTL_15

On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM

Data Transfer Rate: 10.6 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 8, 9 and 10

Bi-Directional Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 14/10/3

Fully RoHS Compliant

Description

DTM64312E is a registered 256Mx72 memory module, which conforms to JEDEC's DDR3, PC3-10600 standard. The assembly is Dual-Rank. Each Rank is comprised of nine 128Mx8 DDR3 Samsung SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology.
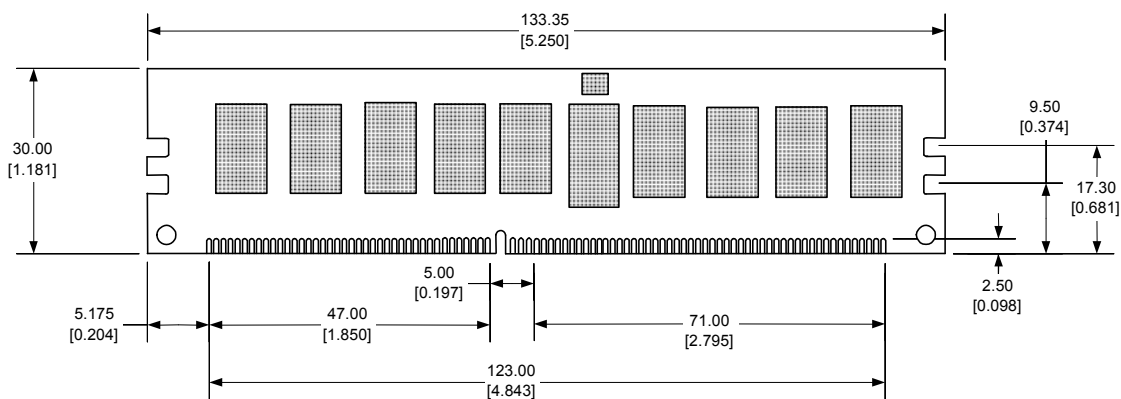
A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.
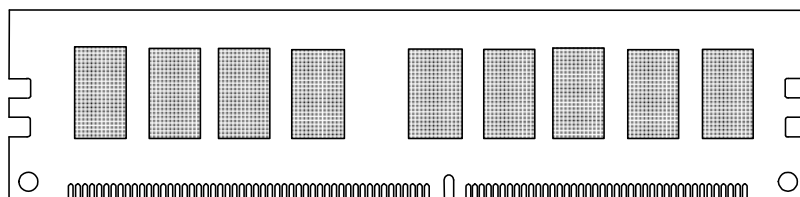
Pin Configuration

Front Side

1 V_{REFDQ}	31 DQ25	61 A2	91 DQ41	
2 V_{SS}	32 V_{SS}	62 V_{DD}	92 V_{SS}	
3 DQ0	33 /DQS3	63 CK1*	93 /DQS5	
4 DQ1	34 DQS3	64 /CK1*	94 DQS5	
5 V_{SS}	35 V_{SS}	65 V_{DD}	95 V_{SS}	
6 /DQS0	36 DQ26	66 V_{DD}	96 DQ42	
7 DQS0	37 DQ27	67 V_{REFCA}	97 /DQ43	
8 V_{SS}	38 V_{SS}	68 P_{AR_IN}	98 DQ48	
9 DQ2	39 CB0	69 VDD	99 DQ48	
10 DQ3	40 CB1	70 A10/AP	100 DQ49	
11 V_{SS}	41 V_{SS}	71 BA0	101 V_{SS}	
12 DQ8	42 /DQS8	72 V_{DD}	102 /DQS6	
13 DQ9	43 DQS8	73 /WE	103 DQS6	
14 V_{SS}	44 V_{SS}	74 /CAS	104 V_{SS}	
15 /DQS1	45 CB2	75 V_{DD}	105 DQ50	
16 DQS1	46 CB3	76 /S1	106 DQ51	
17 V_{SS}	47 V_{SS}	77 ODT1	107 V_{SS}	
18 DQ10	48 V_{TT}	78 V_{DD}	108 DQ56	
19 DQ11	49 V_{TT}	79 /S2, NC*	109 DQ57	
20 V_{SS}	50 CKE0	80 V_{SS}	110 V_{SS}	
21 DQ16	51 V_{DD}	81 DQ32	111 /DQS7	
22 DQ17	52 BA2	82 DQ33	112 DQS7	
23 V_{SS}	53 /E_{RR_OUT}	83 V_{SS}	113 V_{SS}	
24 /DQS2	54 V_{DD}	84 /DQS4	114 DQ58	
25 DQS2	55 A11	85 DQS4	115 DQ59	
26 V_{SS}	56 A7	86 V_{SS}	116 V_{SS}	
27 DQ18	57 V_{DD}	87 DQ34	117 SA0	
28 DQ19	58 A6	88 DQ35	118 SCL	
29 V_{SS}	59 A4	89 V_{SS}	119 SA2	
30 DQ24	60 V_{DD}	90 DQ40	120 V_{TT}	

Back Side

121 V_{SS}	151 V_{SS}	181 A1	211 V_{SS}
122 DQ4	152 DM3	182 V_{DD}	212 DM5
123 DQ5	153 NC	183 V_{DD}	213 NC
124 V_{SS}	154 V_{SS}	184 CK0	214 V_{SS}
125 DM0	155 DQ30	185 /CK0	215 DQ46
126 NC	156 DQ31	186 V_{DD}	216 DQ47
127 V_{SS}	157 V_{SS}	187 /Event	217 V_{SS}
128 DQ6	158 CB4	188 A0	218 DQ52
129 DQ7	159 CB5	189 V_{DD}	219 DQ53
130 V_{SS}	160 V_{SS}	190 BA1	220 V_{SS}
131 DQ12	161 DM8	191 V_{DD}	221 DM6
132 DQ13	162 NC	192 /RAS	222 NC
133 V_{SS}	163 V_{SS}	193 /S0	223 V_{SS}
134 DM1	164 CB6	194 V_{DD}	224 DQ54
135 NC	165 CB7	195 ODT0	225 DQ55
136 V_{SS}	166 V_{SS}	196 A13	226 V_{SS}
137 DQ14	167 NC (TEST)	197 V_{DD}	227 DQ60
138 DQ15	168 /RESET	198 /S3, NC*	228 DQ61
139 V_{SS}	169 CKE1	199 V_{SS}	229 V_{SS}
140 DQ20	170 V_{DD}	200 DQ36	230 DM7
141 DQ21	171 A15	201 DQ37	231 NC
142 V_{SS}	172 A14	202 V_{SS}	232 V_{SS}
143 DM2	173 V_{DD}	203 DM4	233 DQ62
144 NC	174 A12/ /BC	204 NC	234 DQ63
145 V_{SS}	175 A9	205 V_{SS}	235 V_{SS}
146 DQ22	176 V_{DD}	206 DQ38	236 V_{DDSPD}
147 DQ23	177 A8	207 DQ39	237 SA1
148 V_{SS}	178 A6	208 V_{SS}	238 SDA
149 DQ28	179 V_{DD}	209 DQ44	239 V_{SS}
150 DQ29	180 A3	210 DQ45	240 V_{TT}

* Not used

Pin Description

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0], /DQS[8:0]	Differential Data Strobes
DM[8:0]	Data Mask
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S[3:0]	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFDQ}	Reference Voltage for DQ
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
/Event	Temperature Sensing
NC	No Connection

Front view

133.35
[5.250]

30.00
[1.181]

9.50
[0.374]

17.30
[0.681]

5.00
[0.197]

2.50
[0.098]

5.175
[0.204]

47.00
[1.850]

71.00
[2.795]

123.00
[4.843]

Back view
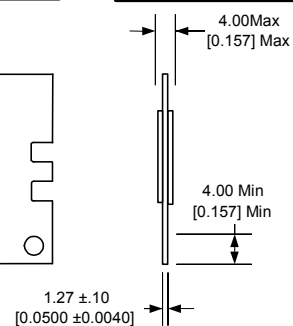
Side view

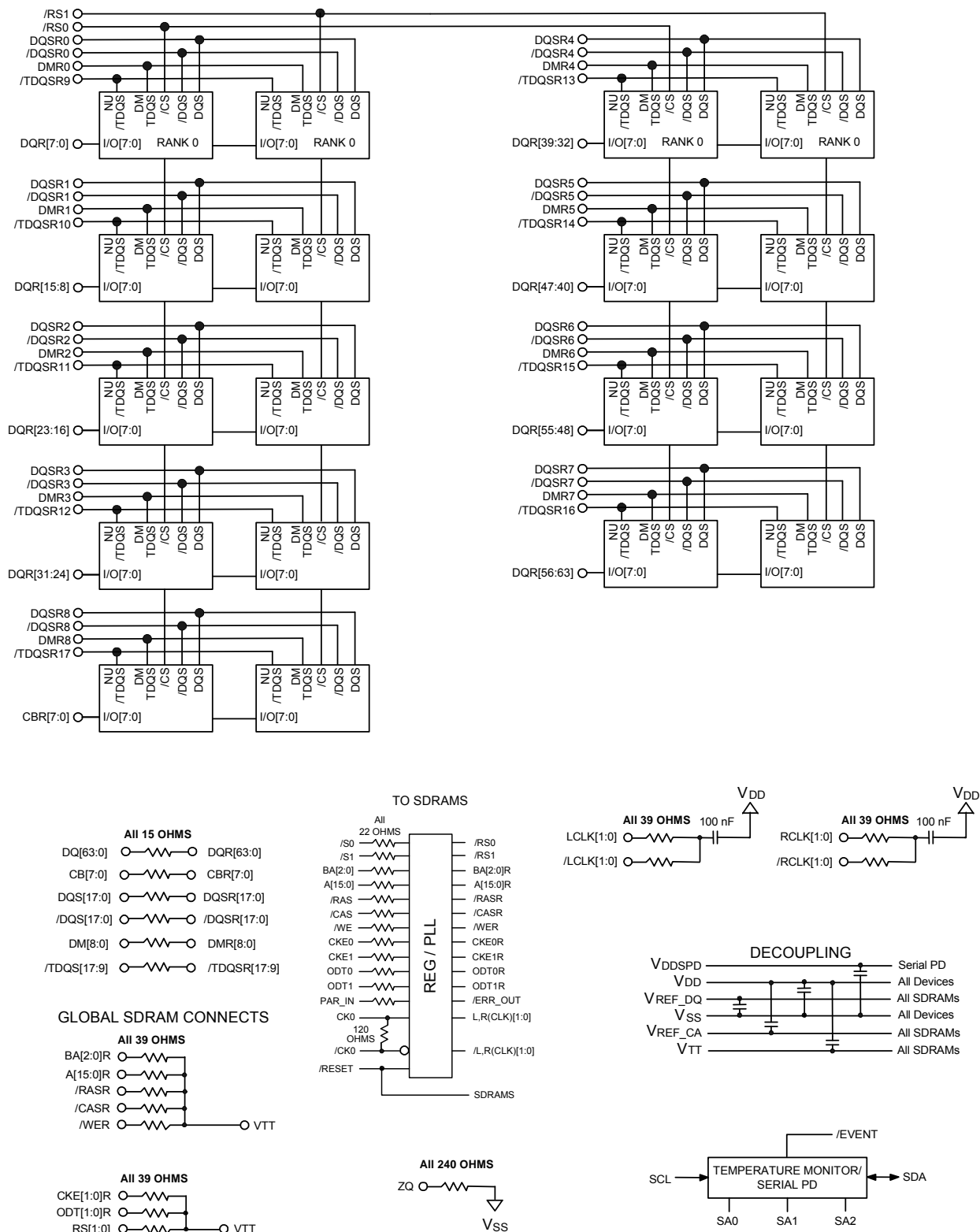4.00Max
[0.157] Max

4.00 Min
[0.157] Min

1.27 ±.10
[0.0500 ±0.0040]

Notes

Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

All dimensions are expressed: millimeters [inches]

Absolute Maximum Ratings
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	T_A	0	70	C
DRAM Case Temperature, Operating	T_{CASE}	0	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V_{REFDQ}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
I/O Reference Voltage	V_{REFCA}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1

Notes:
1) The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value. For Reference V_{DD}/2 ± 15 mV.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	V_{REF} + 0.1	V_{DD}	V
Logical Low (Logic 0)	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.1	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	V_{REF} + 0.175	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	V_{REF} - 0.175	V

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH.DIFF}$	+0.200	DC:V_{DD} AC:V_{DD}+0.4	V
Differential Input Logic Low	$V_{IL.DIFF}$	DC:V_{SS} AC:V_{SS}-0.4	-0.200	V
Differential Input Cross Point Voltage relative to VDD/2	V_{IX}	- 0.150	+ 0.150	V

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	1.5	2.5	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	C_I	1.5	2.5	
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[8:0], /DQS[8:0], DM[8:0], TDQS[17:9]	C_{IO}	3	5	pF
ZQ Capacitance	ZQ	C_{ZQ}	-	6	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < VIN < VDD)	I_{IL}	-18	+18	µA	1,2
Output Leakage Current (0V < VOUT < VDDQ)	I_{OL}	-10	+10	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ, DQS, DQS and ODT are disabled

I$_{DD}$ Specifications and Conditions (T$_A$ = 0 to 70 C, Voltage referenced to V$_{ss}$ = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I$_{DD}$0*	Operating current : One bank ACTIVATE-to-PRECHARGE	1740	mA
Operating One Bank Active-Read-Precharge Current	I$_{DD}$1*	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	1875	mA
Precharge Power-Down Current	I$_{DD}$2P**	Precharge power down current: (Slow exit)	1020	mA
Precharge Power-Down Current	I$_{DD}$2P**	Precharge power down current: (Fast exit)	1290	mA
Precharge Quiet Standby Current	I$_{DD}$2Q**	Precharge quiet standby current	1470	mA
Precharge Standby Current	I$_{DD}$2N**	Precharge standby current	1470	mA
Active Power-Down Current	I$_{DD}$3P**	Active power-down current	1290	mA
Active Standby Current	I$_{DD}$3N**	Active standby current	1740	mA
Operating Burst Write Current	I$_{DD}$4W*	Burst write operating current	2370	mA
Operating Burst Read Current	I$_{DD}$4R*	Burst read operating current	2280	mA
Burst Refresh Current	I$_{DD}$5**	Refresh current	2595	mA
Self Refresh Current	I$_{DD}$6**	Self-refresh temperature current: MAX T$_C$ = 85°C	1020	mA
Operating Bank Interleave Read Current	I$_{DD}$7*	All bank interleaved read current	3225	mA

* One module rank in this operation the rest in IDD2P slow exit.
** All module ranks in this operation.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.5	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.5	1.875	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	65	-	ps
DQ Input Pulse Width	t_{DIPW}	400	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-255	+255	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	30	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	$t_{CK(avg)}$
Clock Half Period	t_{HP}	minimum of t_{CH} or t_{CL}	-	ns
Address and Command Hold Time after Clock	t_{IH}	140	-	ps
Address and Command Setup Time before Clock	t_{IS}	65	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	36	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	49.5	-	ns
RAS-to-CAS Delay	t_{RCD}	13.5	-	ns
Average Periodic Refresh Interval 0° C $\leq$ T$_{CASE}$ < 85° C	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval 0° C $\leq$ T$_{CASE}$ < 95° C	t_{REFI}	-	3.9	µs
Auto Refresh Row Cycle Time	t_{RFC}	110	-	ns
Row Precharge Time	t_{RP}	13.5	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

SERIAL PRESENCE DETECT MATRIX

Byte #	Function.	Value	Hex
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage.		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision.	Rev. 1.0	0x10
2	Key Byte / DRAM Device Type.	DDR3 SDRAM	0x0B
3	Key Byte / Module Type.		0x01
	Bit 3 ~ Bit 0. Module Type -	RDIMM	
	Bit 7 ~ Bit 4. Reserved -	0	
4	SDRAM Density and Banks.		0x02
	Bit 3 ~ Bit 0. Total SDRAM capacity, in megabits -	1Gb	
	Bit 6 ~ Bit 4. Bank Address Bits -	8 banks	
	Bit 7. Reserved -	0	
5	SDRAM Addressing.		0x11
	Bit 2 ~ Bit 0. Column Address Bits -	10	
	Bit 5 ~ Bit 3. Row Address Bits -	14	
	Bit 7, 6. Reserved	0	
6	Reserved.	UNUSED	0x00
7	Module Organization.		0x09
	Bit 2 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	2-Rank	
	Bit 7, 6. Reserved	0	
8	Module Memory Bus Width.		0x0B
	Bit 2 ~ Bit 0. Primary bus width, in bits -	64-Bits	
	Bit 4, Bit 3. Bus width extension, in bits -	8-Bits	
	Bit 7 ~ Bit 5. Reserved -	0	
9	Fine Timebase (FTB) Dividend / Divisor.		0x52
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Divisor	2	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Dividend	5	
10	Medium Timebase (MTB) Dividend.	1 (MTB = 0.125ns)	0x01
11	Medium Timebase (MTB) Divisor.	8 (MTB = 0.125ns)	0x08
12	SDRAM Minimum Cycle Time (tCKmin).	1.5ns	0x0C
13	Reserved.	UNUSED	0x00
14	CAS Latencies Supported, Least Significant Byte.		0x74
	Bit 0. CL = 4 -		
	Bit 1. CL = 5 -		
	Bit 2. CL = 6 -	X	
	Bit 3. CL = 7 -		
	Bit 4. CL = 8 -	X	
	Bit 5. CL = 9 -	X	

	Bit 6. CL = 10 -	X	
	Bit 7. CL = 11 -		
15	CAS Latencies Supported, Most Significant Byte.		0x00
	Bit 0. CL = 12 -		
	Bit 1. CL = 13 -		
	Bit 2. CL =14 -		
	Bit 3. CL = 15 -		
	Bit 4. CL = 16 -		
	Bit 5. CL = 17 -		
	Bit 6. CL = 18 -		
	Bit 7. Reserved.		
16	Minimum CAS Latency Time (tAAmin).	13.5ns	0x6C
17	Minimum Write Recovery Time (tWRmin).	15.0ns	0x78
18	Minimum RAS# to CAS# Delay Time (tRCDmin).	13.5ns	0x6C
19	Minimum Row Active to Row Active Delay Time (tRRDmin).	6.0ns	0x30
20	Minimum Row Precharge Delay Time (tRPmin).	13.5ns	0x6C
21	Upper Nibbles for tRAS and tRC.		0x11
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -	1	
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -	1	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte.	36.0ns	0x20
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte.	49.5ns	0x8C
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte.	110.0ns	0x70
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte.	110.0ns	0x03
26	Minimum Internal Write to Read Command Delay Time (tWTRmin).	7.5ns	0x3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin).	7.5ns	0x3C
28	Upper Nibble for tFAW.		0x00
	Bit 3 ~ Bit 0. tFAW Most Significant Nibble -	0	
	Bit 7 ~ Bit 4. Reserved -	0	
29	Minimum Four Activate Window Delay Time (tFAWmin), Least Significant Byte.	240	0xF0
30	SDRAM Optional Features.		0x02
	Bit 0. RZQ / 6 -		
	Bit 1. RZQ / 7 -	X	
	Bit 6 ~ Bit 2. Reserved -		
	Bit 7. DLL-Off Mode Support		
31	SDRAM Drivers Supported.		0x81
	Extended Temperature Range -	X	
	Extended Temperature Refresh Rate -		
	Auto Self Refresh (ASR) -		
	On-die Thermal Sensor (ODTS) Readout -		
	Reserved -		
	Reserved -		
	Reserved -		

		Reserved -	X	
32	Reserved		€	0x80
33-59	Reserved		UNUSED	0x00
60	Module Nominal Height.			0x0F
	Bit 4 ~ Bit 0. Module Nominal Height max, in mm -		29<h<=30	
	Bit 7 ~ Bit5. Reserved -		0	
61	Module Maximum Thickness.			0x11
	Bit 3 ~ Bit 0. Front, in mm (baseline thickness = 1 mm) -		1<th<=2	
	Bit 7 ~ Bit 4. Back, in mm (baseline thickness = 1 mm) -		1<th<=2	
62	Reference Raw Card Used.			0x01
	Bit 4 ~ Bit 0. Reference Raw Card -		R/C B	
	Bit 6, Bit 5. Reference Raw Card Revision -		Rev.0	
	Bit 7. Reserved -		0	
63	Address Mapping from Edge Connector to DRAM.			0x05
	Bit 0. Rank 1 Mapping (Registered DIMM - Reserved) -			
	Bit 7 ~ Bit 1. Reserved -			
64-66	Module-Specific Section		UNUSED	0x00
67	Register Revision Number			FF
68, 69	Module-Specific Section		UNUSED	
70	Module-Specific Section		P	0x50
71-112	Module-Specific Section		UNUSED	0x00
113	Module-Specific Section.		UNUSED	0x00
114-116	Module-Specific Section		UNUSED	0x00
117	Module Manufacturer ID Code, Least Significant Byte			0x01
118	Module Manufacturer ID Code, Most Significant Byte			0x91
119	Module Manufacturing Location		UNUSED	0x00
120, 121	Module Manufacturing Date			0x20
122-125	Module Serial Number			0x20
126	Cyclical Redundancy Code (CRC).		CRC	0xB4
127	Cyclical Redundancy Code (CRC).		CRC	0xEA
128-131	Module Part Number			0x20
132	Module Part Number		D	0x44
133	Module Part Number		A	0x41
134	Module Part Number		T	0x54
135	Module Part Number		A	0x41
136	Module Part Number		R	0x52
137	Module Part Number		A	0x41
138	Module Part Number		M	0x4D
139	Module Part Number			0x20
140	Module Part Number		6	0x36

141	Module Part Number	4	0x34
142	Module Part Number	3	0x33
143	Module Part Number	1	0x31
144	Module Part Number	2	0x32
145	Module Part Number		0x20
146, 147	Module Revision Code		0x20
148	DRAM Manufacturer ID Code, Least Significant Byte	UNUSED	0x00
149	DRAM Manufacturer ID Code, Most Significant Byte	UNUSED	0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00

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